SPECIFICATION

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[Method of clock recovery in a TMDS repeater.]

Background of Invention

[0001] 1.Technical Field.

[0002] The present invention relates to computer systems in general and, more particularly, to a transmission of a TMDS coded serialized video data over long lines to a plurality of TMDS receivers, integrated into video display devices.

[0003] 2.Related Art.

[0004] A prior art high speed serial video signal transmission system, described in the US patent number 5,974,464, comprises a graphic controller, video transmitter, 3 pairs of data wires and 1 pair of clock wires forming a TMDS line, video receiver and LCD panel as a display device. The above structure is shown in FIG.1.

[0005] Nowadays computer systems with a plurality of video displays are widely used. An example of a computer system shows the same content on a plurality of video displays is a public presentation system that can be used during conferences, public events, or in purposes of public information or commercial purposes. Video displays in a such kind of a public broadcasting system usually are located far from a video source computer.

[0006] The prior art system described above, however, allows one display device with a TMDS receiver for one computer with a TMDS transmitter with a limited length of a TMDS line comprising 3 pairs for data and 1 pair for clock.

[0007] In order to connect several video displays to a computer over a TMDS line it is possible to build a repeater comprising one TMDS receiver and several TMDS

transmitters. However, several of the said above repeaters, connected in serial in order to extend TMDS line length or increase amount of connected video displays, cause visible distortion of a displayed video because of accumulation of phase distortions happened in cables, receivers and transmitters.

Summary of Invention

[0008] It is an object of the present invention to provide a method of clock recovery in a transition minimized differential scaling (TMDS) digital transmission systems. This method allows building a TMDS repeater comprising one TMDS receiver, one or more TMDS transmitters and a recovery circuit that reconstructs original video data signal and does not accumulate phase distortions happened in cables, receivers and transmitters.

[0009] The recovery method is based on using a quartz clock for TMDS transmitters instead of the clock received over a TMDS line. A dual port first-in-first-out (FIFO) memory is used for buffering data from a TMDS receiver to TMDS transmitters. It is necessary to use the said FIFO memory buffer because the clock obtained from a quartz oscillator onboard a repeater cannot exactly match frequency and phase of a clock received over TMDS line by a TMDS receiver.

[0010] Digital video signal over TMDS line has a data disable interval between lines of video data. During this interval no high-speed video data is transmitted, but only low frequency signals of vertical and horizontal synchronization and optional control signals. Time to receive a line of digital video data depends on the received TMDS clock frequency and is different from time to transmit the same line of video data, which depends on a quartz oscillator clock frequency. Time from a data disable interval is used to compensate the said above time difference and FIFO memory is used to buffer a portion of digital video data line. In principle, the said time difference cannot be longer than time of a data disabled interval.

Brief Description of Drawings

[0011] FIG.1 is a block diagram of a prior art system.

[0012] FIG.2 is a block diagram of a typical public broadcasting system.

[0013] FIG.3 is a block diagram of a repeater based on a prior art system.

[0014] FIG.4 is a block diagram of a repeater with a clock recovery circuit.

[0015] FIG.5 is a flowchart of the operation of a control unit.

Detailed Description

[0016] FIG.1 illustrates a prior art system that comprises a graphic controller 11 and TMDS transmitter 12, both located in a computer 21, as well as TMDS receiver 13 and LCD panel 14, located in a digital display device 23. Digital video data is transmitted from a computer 21 to a digital display device 23 though a TMDS line 24 that usually comprises 3 pairs for data and one pair for clock.

[0017] TMDS transmitter 12 during data enable interval, when data enable (DE) signal 16 is high, serializes active video data 15 obtained from a graphic controller 11 though 24 or 32 conductor wires. During data disabled interval, when DE signal 16 is low, TMDS transmitter encodes and serializes control signals 18. All the mentioned signals are sampled according to a pixel clock 10 from a graphic controller 11.

[0018] TMDS receiver 13 de-serializes active video data during data enable interval and de-serializes and decodes control signals during data disable interval. Also TMDS receiver 13 reconstructs a pixel clock. However, compare to the original pixel clock 10, received TMDS clock 17 has a jitter and phase distortion, that limits the further use of this clock.

[0019] FIG.2 illustrates an example of the desired public digital video data broadcasting system, where a plurality of digital display devices 23 displays a video content obtained from a computer 21 via a TMDS lines 24. Repeaters 22 are used to receive TMDS data and re-transmit it to a plurality of digital display devices.

[0020] FIG.3 is a block diagram of a repeater 22A without clock recovery circuit. In this repeater, data de-serialized by a TMDS receiver 13 is shared between several TMDS transmitters 12. All the TMDS transmitters 12 use received TMDS clock 17 with jitter and phase distortion to generate internal serial data clock, which has 10 times higher frequency. Further transmission of a TMDS clock 17 and repeating it by the next repeaters 22A cause a visible distortion of a displayed video due to accumulation of

phase distortions happened in cables, receivers and transmitters.

[0021] FIG.4 is a block diagram of a repeater 22B with a clock recovery circuit. TMDS receiver 13 receives a serial digital video data over a TMDS line 24. TMDS receiver 13 outputs parallel video data 15, control signals 18 after de-serializing, as well as TMDS clock 17 and data enable (DE) signal 16. FIFO memory 41 is used to buffer active video data. Control unit 44 generates read enable (RE) signal 45, which is used by a FIFO memory 41 and is used by TMDS transmitters 12 as an outgoing data enable signal. Quartz oscillator 42 provides quartz clock 43 for sampling an outgoing active video data 46, outgoing control signals 48 and RE signal 45. Optional unit 49 is used to reconstruct a signal of a horizontal video synchronization.

[0022] As shown in FIG.4 clock is recovered by a very simple method, just by generating a new clock by a quartz oscillator. However this simple method of clock recovery requires data buffering due to the difference in phase and frequency between incoming TMDS clock and quartz clock. Unit 44 performs control of data buffering.

[0023] Control unit 44 has 3 input signals: data enable 16, incoming TMDS clock 17 and quartz clock 43. According to the given signals, control unit 44 generates a read enable (RE) signal 45 that is used as a signal to enable data read from FIFO memory and at the same time it is a data enable signal for TMDS transmitters 12.

[0024] FIG.5 is a flowchart of the operation of a control unit 44. As shown in a flowchart, unit 44 enables data read (RE) from FIFO memory only after N rising edges of an incoming TMDS clock. At this moment FIFO memory 41 stores N pixels of an active video data. Each rising edge of an incoming TMDS clock 17 stores a pixel data into a FIFO memory 41 and increases a counter in a control unit 44. Each rising edge of a quartz clock 43 reads a pixel from a FIFO memory 41 and decreases a counter in a control unit 44. When a counter reaches zero value, RE signal 45 goes low, disabling data read from a FIFO memory 41 and disabling outgoing TMDS data until the next rising edge of an incoming DE signal 16 and buffering of N pixels of the next video line.

[0025] The value N depends on a maximum desired frequency tolerance of a quartz clock 43 from an incoming TMDS clock 17. Also the value N defines the required size of a

FIFO memory 41. In order to illustrate the operation principle of a control unit 44 and provide guidance for choosing value N there is an example given below.

[0026] For example, for popular computer screen resolution of 768 lines per 1024 horizontal pixels, each line of digital video data consists of an active video data of 1024 pixels and a video blanking period of 320 pixel clocks. Data enable period (DE signal is high) is an active video data period. Data disable period (DE signal is low) is a video blanking period.

[0027] Usually clock of 66 MHz is used as a pixel clock for a given above resolution. Assume that the frequency tolerance of the used quartz clock is as big as 100 kHz. That means, that in the worst cases it can as less as 65.9 MHz or as much as 66.1 MHz instead of the desired 66.0 MHz.

[0028] Assume that in the first worst case the input TMDS clock 17 frequency is 65.9 MHz and the frequency of the quartz clock 43 is 66.1 MHz. According to the given frequencies the length of data enabled period (DE is high) for incoming video data is equal to 15539 nanoseconds and the length of Data Enable period for outgoing video data is equal to 15492 nanoseconds. Based on the above calculations, transmission time of the outgoing active video line data is 47 nanoseconds less than receiving time of the incoming active video line data. For the given clocks frequencies, 47 nanoseconds is time for the transmission of less than 4 pixels. Thus the value of N can be chosen equal to 4. That means that 4 pixels of an active video data will be buffered in a FIFO memory before TMDS transmitters 12 will begin to transmit the outgoing active video data. As a quartz clock in given case is faster than incoming TMDS clock, at the falling edge of an incoming DE signal a FIFO memory will buffer only one the last pixel data, which will be transmitted out during the next period of a quartz clock.

[0029] In the second worst case the input TMDS clock 17 frequency is 66.1 MHz and the frequency of the quartz clock 43 is 65.9 MHz. Transmission time of the outgoing active video line data is 47 nanoseconds longer than receiving time of the incoming active video line data. Thus at the falling edge of an incoming DE signal a FIFO memory will buffer data of the last 8 or 9 pixels. Transmission of an active video line data will be complete during the next 8-9 periods a quartz clock.

[0030] Optional unit 49 can be used for the recovery of control signals. Control signals usually include a horizontal synchronization signal, a vertical synchronization signal and several signals for a general purpose control. Control signals are valid only during data disabled interval. Because of a clock recovery described above, the outgoing data disabled interval can have a period different from a period of the incoming data disabled interval and outgoing control signals 48 should be sampled according to the recovered quartz clock.

[0031] Usually general-purpose control signals are specified not to have any signal transitions during data disabled interval. This allows direct bypass of all incoming general-purpose control signals to TMDS transmitters 12.

[0032] One-pixel jitter of a vertical synchronization signal usually does not cause a video picture distortion on screen of a target display device. This allows direct bypass of a vertical synchronization signal to TMDS transmitters 12.

[0033] A jitter of a horizontal synchronization signal can cause a video picture distortion on screen of a target display device when the said display device requires a horizontal synchronization signal. Nowadays a plurality of digital display devices use only data enable signal for synchronization purposes and make no use of horizontal or vertical synchronization signals. However, when a stable horizontal synchronization signal is required, an optional unit 49 can reproduce it.

[0034] Use of the described above TMDS repeater with a clock recovery circuit allows building a public digital video data broadcasting system, where is no principle limitations for the quantity of display devices and the length of TMDS data line.